Applicant : Gilbert Wolrich et al.   Attorney's Docket No.: 10559-305US1 / P9626US
Serial No. : 10/069,229
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REMARKS

Claims 1, 14, 17 and 20 were amended to correct typographical errors. Claim 20 was also amended for clarity and to form a proper antecedent basis for the wording "branch instruction."

The examiner rejected claims 1-3, 6, 10, 13-21 under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,724,521 to Carron et al. Independent claim 1 recites "a branch instruction that causes a processor to branch from executing a first sequential series of instructions to a different sequential series of instructions based on a byte in a register being equal or not equal to a specified byte value, if the specified byte matches or mismatches the byte value."

In contrast, none of Carron's various branch (BRANCH) and compare (COMP) instructions disclosed in the "Alphabetic Listing of Commands" in Section 4 of Table I (col. 117 to col. 176) describes an instruction that performs a branching based on a byte in a register being equal or not equal to a specified byte value, as required by applicant's claim 1. Rather, as stated, for example, in col. 134, lines 31-31, the effect of the COMP_CHAR command is to: "Compare byte at specified position in the *designated buffer* with the byte constant in the command" (emphasis added). Thus, what the COMP_CHAR command compares is a command operand value to a value held in a buffer location (e.g., a RAM location), not in a processor's register.

The Examiner also rejected Claims 4 and 5 under 35 U.S.C. 103(a) as being unpatentable over Carron in view of Atkins et al, U.S. Patent No. 5,898,866; Claims 7, 8, and 11 under 35 U.S.C. § 103(a) as being unpatentable over Carron in view of Bruckert et al, U.S. Patent No. 4,742,151; Claim 9 under 35 U.S.C. § 103(a) as being unpatentable over Carron in view of Gusefski et al, U.S. Patent No. 5,202,972 and Claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Carron in view of Grochowski et al, U.S. Patent No. 5,442,756.

Claims 2-13 depend from independent claim 1. Accordingly, claims 2-13 are patentable for at least the same reasons as claim 1.

Additionally, the examiner admits, with respect to claim 12, that "Carron does not teach the instruction of claim 1 wherein the branch instruction branches on a byte not matching the

byte value and wherein the instruction prefetches the next sequential instruction" (paragraph 28, page 7 of the May 20, 2005, Office Action). The examiner, however, argues that U.S. Patent No. 5,442,756 to Grochowski teaches this feature.

Applicant's claim 12 discloses that a decision to branch may be taken "on a byte not matching the byte value."

Grochowski discloses apparatus and method for improving the performance of superscalar pipelined computers using branch prediction and verification that the predicted branch is correct. The examiner points to col. 9, lines 1-3, and col. 2, lines 57-61, as showing that Grochowski discloses branching on a first byte value not matching a second byte value. But these paragraphs merely discuss the use of a general branch predicting scheme and/or the motivation for using such a scheme, and do not discuss the use of branch instructions per se. Particularly, Grochowski describes that when performing the predictive branching scheme, the scheme first determines if the instruction to be branched to is present in the branch target buffer 32 (col. 8, line 65 to col. 9, line 3). If the instruction to be branched to is not already in the branch target buffer, predictive branching is not used. Nowhere, however, does Grochowski describe the use of an instruction, let alone a branch instruction, that causes branching to another part of the program upon one byte value not matching a second byte value, as required by applicant's claim 12.

Claim 14 describes a computer program product featuring "determine whether the byte in the register is equal or not equal to a specified byte value contained in the instruction." For similar reasons as those provided with respect to claim 1, at least this feature is neither described nor suggested by the art. Claims 15-16, which depend from claim 14, are patentable for at least the same reasons as claim 14.

Claim 17 describes a processor featuring "determine whether the byte in the register is equal or not equal to a specified byte value contained in the instruction." For similar reasons as those provided with respect to claim 1, at least this feature is not disclosed by the art. Claims 18-19, which depend from claim 17, are patentable for at least the same reasons as claim 17.

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Claim 20 describes a method featuring "determining whether the byte in the register is equal or not equal to a specified byte value contained in the instruction." For similar reasons as those provided with respect to claim 1, at least this feature is not disclosed by the art. Claim 21, which depends from claim 20, is patentable for at least the same reasons as claim 17.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges to deposit account 06-1050, referencing attorney docket 10559-305US1.

Respectfully submitted,

Date: July 25, 2005

Ido Rabinovitch
Reg. No. L0080

PTO Customer No. 26161
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

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